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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,274	08/07/2001	Paul Metzgen	174/221	4898

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/924,274	METZGEN, PAUL	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 23-29* is/are rejected.

7)☒ Claim(s) *29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/10/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 09/924,274 and amendment filed on 8/10/2006. Election without traverse of Claims 1-6 and cancellation of withdrawn claims 7-22 are acknowledged. Thus claims 1-6 and newly added claims 23-30 remain pending in the application.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-6 and 23-28 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-4, 6-8, 10-11, 13-17, 19, 21-23, 25-26 and 27 of copending Application No. 09/924,272. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant application and the copending application claim the same subject matter of optimizing a circuit using software-to-hardware compiler, where an optimized circuit is generated using a software-to-hardware compiler at a later stage of the compilation. Although, the copending application does not disclose analyzing a

circuit, it would been obvious to practitioners the art because the analyzing circuit and optimizing the circuit by modifying the software of the program would effectively optimizing the circuit to thereby generate the optimized circuit as implemented.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-6 and 23-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Agarwal et al. (5,761,484).

6. As to claims 1 and 23, Agarwal et al. teach a compilation technique to overcome device pin limitations using virtual interconnections. The virtual interconnections are established by software or hardware compiler programs between programmable logic devices (col. 2 lines 36-51). A virtual interconnection represents a connection from logical output one programmable logic device to a logical input of another programmable logic device. The resulting improvement in bandwidth reduced the need

for global routing allowing effective use of low dimension inter-chip connections (such as nearest-neighbor). The software compiler utilizes static routing or dynamic routing and relies on minimum hardware support (col. 2 lines 1-67, col. 12 lines 1-15). The establishment of virtual interconnections corresponds to establishment of communications between the programmable logic circuit and a least one software device. Agarwal et al. suggest the method of optimizing the circuit using virtual interconnections between programmable logic devices provides mapping efficiency (col. 9 lines 61-67) and using timing and/or locality sensitive partitioning with virtual interconnections has potential for reducing the required number routing sub-cycles. The communication bandwidth can be further increased with pipeline compaction, a technique of overlapping the start and end of long virtual path with shorter paths traveling in the same direction. A more robust implementation of virtual interconnections replaces the global barrier imposed by routing phases with a finer granularity of communication scheduling, possible overlapping computation and communication as well (col. 11 lines 55-67, col. 12 lines 1-6). Note that logical inputs and logical outputs corresponding to software portion that is used to establish virtual interconnections (communications) as claimed (Fig. 3). Thus, Agarwal et al. teach determining whether to splitting the program into a hardware portion and software portion because Agarwal et al. teach using compiler to establish virtual interconnections using existing hardware portion of the programmable logic circuit for optimizations of the circuit. Since, the establishment of virtual interconnections has been modified by changing logical

inputs/outputs for optimizations, Agarwal et al. teach modifying the software portion of the program.

7. As to claim 2 and 24, Agarwal et al. teach using software-to-hardware compiler to analyze the circuit at a later stage in a compilation (col. 2 lines 65-67).

8. As to claim 3 and 25, Agarwal et al. teach analyzing the circuit's critical path (col. 2 lines 65-67, col. 7 lines 31-50).

9. As to claim 4-5 and 26-27, Agarwal et al. teach placing at least one register and at least one FIFO in the circuit (col. 7 lines 30-37; col. 7 lines 58-67; col. 8 lines 1-46; col. 9 lines 1-23; Figs. 3, 6).

10. As to claim 5 and 28, Agarwal et al. teach placing at least one interface buffer in the circuit (Fig. 7).

11. Claims 1 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Shyr (6,871,341 B1).

12. As to claims 1 and 23, Shyr teaches a method using software-to-hardware compiler for optimizing a programmable logic circuit. The method comprises prior to execution of a software program, code segments identified as Hard Functions are implemented for a) Soft Execution and b) Hard Execution. The portions of the code, marked fro hardware acceleration, executed outside of the embedded processor and in reconfigurable logic. Meanwhile, each section of code marked for hardware acceleration is transcribed to its functional equivalence in logic in the form of configuration bits. The configuration bits stored in the configuration memory can configuration the reconfiguration logic to perform exact function of the section code they

were transcribed from. With this duality in implementation the system can invoke software execution as an alternative, in case of the configuration bits associated with a function is not readily in place for execution when the function is called. As the result, the system will never have to stall (at least see col. 3 lines 15-49; col. 6 lines 6-35; col. 7 lines 27-67).

13. As to claims 2-6 and 24-28, Shyr teach the claim limitations using a compiler to analyze the programmable logic at later stage in a compilation, analyzing the programmable logic circuit's critical path and optimizing the programmable logic circuit by placing at least one register, one FIFO and interface buffer in the programmable logic circuit (see at least col. 9 lines 1-67; col. 10 lines 1-67; col. 14 lines 9-61).

Remarks

14. Applicants argued that Agarwal et al. do not appear to teach determining whether to split the program into a hardware portion and a software portion and modifying the programmable logic circuit to executing portion the software portion of the program. Examiner disagrees. The reasons are clearly described in the above rejection. Regarding to doubling patenting rejection, these two applications have filed on the same date. The double patenting is only remained in this application when other application has been indicated allowance. Therefore, a terminal disclaimer is required.

Allowable Subject Matter

15. Claims 29- and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does

not teach or fairly suggest modifying the programmable logic circuit comprising removing the software portion of the program from the programmable logic circuit.

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER